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EXAMINER
MASKULINSKI, MICHAEL C

ART UNIT	PAPER NUMBER
2184	14

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/410,642	EDWARDS ET AL.	
	Examiner	Art Unit	
	Michael C Maskulinski	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 11-13, 15-18, 20-22, and 25-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Wolff et al., U.S. Patent 4,486,826.

Referring to claims 1, 22, 33, and 34:

a. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an address (packet routing information).

b. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an identical set of cycle definition, address, data, parity and other signals that can be compared to warn of erroneous information transfer between units (packets of information, wherein each packet comprises a number of fields containing information).

c. In column 2, lines 31-35, Wolff et al. disclose a computer system (a functional circuit), which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure which provides all information transfers between the several units of the module (interconnect for information transfer).

d. In column 2, lines 31-35, Wolff et al. disclose that the computer system has a single bus structure, which provides all information transfers between the several units of the module (circuitry for receiving at least part of said information).

e. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions).

f. In column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions).

Referring to claim 2, in column 11, lines 36-54, Wolff et al. disclose that in response to the fault signal, the control section produces an error signal (trace message) that the X bus transmits to all units of the module.

Referring to claims 3 and 4, in column 11, lines 50-54, Wolff et al. disclose that any failing unit also produces an interrupt signal that causes the central processing unit of the module (one or more CPUs) to interrogate the different units to locate the faulty one.

Referring to claim 5, in column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (prevent one or more modules from being granted access to the interconnect).

Referring to claims 6 and 11, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a broken flip-flop to disable the drivers of a peripheral device in response to a fault.

Referring to claim 12, in column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator).

Referring to claims 13 and 15, in column 25, lines 32-40, Wolff et al. disclose that the central processing unit (circuit) has two subsystems and control circuits within the unit that take the unit off-line upon detection of an error (precondition: enabled or not enabled). Further, in column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator).

Referring to claims 16 and 17, in figures 5A, 5B, and 1, and in column 28, lines 21-35, Wolff et al. disclose latch 120 which is between the interconnect and the processor module (circuitry external to said circuit). The latch provides temporary storage of output data so that in the event any error is reported on the buses, the operating sequence in which the error was reported can be duplicated and the data retransmitted on the A bus 42 (external circuitry is enabled).

Referring to claims 18, 20, and 21, in column 3, lines 57-68, Wolff et al. disclose that the bus carries cycle-definition (type of transaction to which the information relates), address (address of the information), data, parity, and other signals that can be compared to warn of erroneous information transfer between units (match conditions). The information comprising packets of information, requests, and response is inherent to the information mentioned above that is sent over a bus.

Referring to claim 25, in column 20, lines 35-55, Wolff et al. disclose an arbitration network (arbiter) which provides an automatic hardware determination of which unit, or pair of partner units, that requests access to the bus structure (interconnect) has priority to initiate an operating cycle (granted access).

Referring to claim 26, in column 20, lines 35-55, Wolff et al. disclose that the processor module (determining circuitry) has two arbitration networks (arbiter) connected to bus A and bus B.

Referring to claims 27 and 31, in column 3, lines 34-47, Wolff et al. disclose that upon detection of an error-manifesting fault in any unit, that unit is isolated and placed off-line so that it cannot transfer information to other units of the module. The partner of

the off-line unit continues operating and thereby enables the entire module to continue operating, normally with essentially no interruption.

Referring to claim 28, in the abstract, Wolff et al. disclose a bus.

Referring to claims 29, 30, and 32, in column 2, lines 48-63, Wolff et al. disclose error detectors (debug module) at the level of each functional unit (module). Further, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator, which switches a so-called broken flip-flop to disable the drivers upon detection of an error (circuitry for performing at least one action). The comparator is part of the control unit, which is part of the functional unit (circuitry in said debug module).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S Patent 4,486,826 as applied to claim 6 above, and further in view of Cepulis, U.S. Patent 6,055,596.

Referring to claim 7, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a so-called broken flip-flop to disable the drivers of a peripheral device (module) in order to prevent it from putting further information onto the bus

(interconnect). However, Wolff et al. don't explicitly disclose using a register for preventing a module from putting information onto the interconnect. In column 75, lines 3-10, Cepulis discloses that the CPU can power up one of the slots by writing a "1" to a corresponding bit of a slot enable register and disable the slot by writing a "0" to this bit. It would have been obvious to one of ordinary skill at the time of the invention to include the slot enable register of Cepulis into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because as disclosed by Wolff et al. a switching means is needed to disconnect a peripheral device. The slot enable register of Cepulis is one type of switching means used to disconnect a peripheral device.

Referring to claim 8, in column 75, lines 3-10, Cepulis discloses that the CPU can power up one of the slots by writing a "1" to a corresponding bit of a slot enable register and disable the slot by writing a "0" to this bit (the register comprises one bit for each module and the value of said bit determines if the respective module is prevented from putting further information into the interconnect).

Referring to claim 9, in column 75, lines 3-10, Cepulis discloses that the CPU (one module arranged to access the register non-intrusively) can power up one of the slots by writing a "1" to a corresponding bit of a slot enable register and disable the slot by writing a "0" to this bit.

Referring to claim 10, in column 75, lines 3-10, Cepulis discloses a slot enable register with a corresponding bit for each slot (the location being independent of the address of the module).

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 13 above, and further in view of Ardini, Jr. et al., U.S. Patent 4,918,693. In column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator). However, Wolff et al. don't explicitly disclose satisfying a precondition by having match conditions occurring a predetermined number of times. In column 8, lines 9-14, Ardini, Jr. et al. disclose a diagnostic program that, after a certain number of parity error signals are received from board 202, it will send a code to disable the parity check circuit output. It would have been obvious to one of ordinary skill at the time of the invention to include the parity error signal threshold of Ardini, Jr. et al. into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because a parity check circuit can become faulty so that it continuously generates a parity error signal on its output (see Ardini, Jr. et al.: column 8, lines 7-9). In this case, to check for a faulty parity circuit would require a precondition.

6. Claims 19 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 1 above, and further in view of Pizzica, U.S. Patent 5,652,754.

Referring to claims 19 and 35, in column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a

processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions). Further, in column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an identical set of cycle definition, address, data, parity and other signals that can be compared to warn of erroneous information transfer between units (packets of information). However, Wolff et al. don't explicitly disclose storing circuitry to store the information which satisfies the at least one condition. In column 2, lines 53-60, Pizzica discloses a signature storage device that stores a fault free signature from a functional digital module and faulty signatures obtained by shorting and opening each of the circuit nodes thereof. It would have been obvious to one of ordinary skill at the time of the invention to include the faulty signature storing of Pizzica into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because *the recorded signatures can be used for subsequent pass/fail determination of digital modules that are tested* (see Pizzica: column 1, lines 46-48).

Further, referring to claim 35:

a. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an address (packet routing information).

b. In column 2, lines 31-35, Wolff et al. disclose a computer system, which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus

structure which provides all information transfers between the several units of the module (interconnect for information transfer).

c. In column 2, lines 31-35, Wolff et al. disclose that the computer system has a single bus structure, which provides all information transfers between the several units of the module (circuitry for receiving at least part of said information).

d. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions).

7. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 22 above, and further in view of Bershteyn et al., U.S. Patent 5,678,028.

Referring to claim 23, in the abstract, Wolff et al. disclose a fault-tolerant computer system comprising a processor unit, a memory unit, one or more peripheral control units, and a bus structure. However, Wolff et al. don't explicitly disclose that these circuits are an integrated circuit. In the Background of Bershteyn et al., a system-on-a-chip debugger is disclosed. It would have been obvious to one of ordinary skill at the time of the invention to make the system of Wolff et al. into the system-on-a-chip debugger of Bershteyn et al. into the. A person of ordinary skill in the art would have

been motivated to make the modification because an entire system can be fabricated on a single wafer decreasing the cost of the entire system (see Bershteyn et al.: column 1, lines 45-67).

Referring to claim 24, in the abstract Wolff et al. disclose a computing module (external module), one or more peripheral control units (modules), and a bus structure (interconnect).

8. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826, and further in view of Merrill et al., U.S. Patent 4,942,552.

Referring to claim 36:

a. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an identical set of cycle-definition, address, data, and parity signals. However, Wolff et al. don't explicitly disclose having fields/signals that contain information including a source field, a transaction type field, a transaction identifier field, and an operation code field. In column 7, lines 26-30, Merrill et al. disclose that both the read commands and the write commands contain parameters which specify the data to be moved, including the source address, destination address, and the length of data to be moved. In column 19, lines 42-50, Merrill et al. disclose an ID field that contains an operation code which identifies one command message from said predetermined set of command messages. In column 23, lines 22-25, Merrill et al. disclose remote command messages including at least first and second remote command message types. In column 11, lines 18-21, Merrill et al. disclose a transaction number that is

included in both the output message and the reply to match up the commands and responses. It would have been obvious to one of ordinary skill at the time of the invention to include the fields of Merrill et al. into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because these fields can be used to in comparison to other signals so as to warn of erroneous information transfer between units (see Wolff et al.: column 3, lines 63-64).

b. In column 2, lines 31-35, Wolff et al. disclose a computer system (a functional circuit), which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure which provides all information transfers between the several units of the module (interconnect for information transfer that is not a circuit-switched bus).

c. In column 2, lines 31-35, Wolff et al. disclose that the computer system has a single bus structure, which provides all information transfers between the several units of the module (circuitry for receiving at least part of said information).

d. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for

determining if said at least part of said information satisfies one or more conditions).

e. In column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions).

Response to Arguments

9. Applicant's arguments filed February 24, 2003 have been fully considered but they are not persuasive.

10. On page 4, under the section A. Rejections under 35 U.S.C. 102, the Applicant argues, "The Wolff et al. reference shows two parallel busses which deliver a "set" of signals. This set of signals would not be confused as a packet by anyone of skill in the art of data communication. This set of signals is akin to a circuit-switched connection in which a circuit connection is made between communicating ends of the bus. The signals in Wolff et al. are not transmitted as a unit as each member of the "set", by design and necessity, travels on a separate signal line. Line noise, switching errors, voltage errors, and the like may affect on member of the set without impacting any other member of the set." The Examiner respectfully disagrees. **Anyone of skill in the art of data communication** knows that a packet in its broadest definition is *a unit of data of some finite-size that is transmitted as a unit* (see IEEE 100 The Authoritative

Dictionary of IEEE Standards Terms, Seventh Edition). Further, the Examiner realizes that the Applicant relies on a definition of packet as defined by Newton's Telecom Dictionary, 18th Edition (2002), on page 4 of the arguments. However, this definition is one of many definitions for a packet and is not the broadest accepted meaning. Also, the definition of packet as given by Applicant is for a network. A network is **not** claimed in any of the claims. Still, further the Applicant **assumes** that "the signals in Wolff et al. are not transmitted as a unit as each member of the "set", by design and necessity, travels on a separate signal line." The Examiner requests that the Applicant show where in Wolff et al. separate signal lines is taught. In the Abstract, Wolff et al. disclose a bus structure common to all units. This is not necessarily separate signal lines. Further, for the sake of argument, even if the bus of Wolff et al. was composed of separate signal lines, the data would still be transmitted in parallel and received at the receiving end as one unit.

11. On page 4, under the section A. Rejections under 35 U.S.C. 102, the Applicant argues, "Packet routing information, described generally at page 5 of the specification, is believed to be a particular type of information that does not appear in a bus-type interconnect of the Wolff reference. The set of signals in Wolff et al. is not routed—it is coupled end-to-end by the physical interconnect. The set of signals in Wolff et al. do not contain routing information as there is but one source and one destination possible. The set of signals in Wolff et al. is not a unit of data; it is a collection of separate signals. Accordingly, Wolff et al. do not show a packet as called for in the claims. At least this feature of the independent claims is not shown or suggested in the Wolff et al.

reference." The Examiner respectfully disagrees. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an address (packet routing information). Further, the Examiner requests that the Applicant show in Wolff et al. where "there is but one source and one destination possible." In Figure 1, Wolff et al. shows **more than one** device connected to the busses. How can there be but one source and one destination?

12. On page 5, under the section A. Rejections under 35 U.S.C. 102, the Applicant argues, "In Wolff et al., the size of the set of information is determined by the number of signal lines in the bus, and not by a protocol used. In contrast, the claims call for packets of information in the ordinary meaning of that term where the packet size is determined by a protocol choice, not a hardware limitation." The Examiner will not address this argument because simply put, the claims **do not** claim a protocol and the argument is irrelevant to the claim language, which is simply a **packet**. The Examiner has given the term packet its broadest possible definition. Further, the Applicant argues, "The patent office itself recognizes in the Manual of Classification that packet switching is a distinct, defined type of switching that is different from circuit switched type connections as shown in the applied reference." Again, the Applicant's argument will not be addressed because it is irrelevant to what is claimed, which is a **packet**.

13. On page 5, under the section A. Rejections under 35 U.S.C. 102, the Applicant argues, "Wolff et al. do not monitor information from the interconnect as that term is used in the instant application. The office action appears to dismiss this limitation of the claims by simply rebutting that this is merely a general allegation that the claims define

a patentable invention. However, this is not merely a general allegation: specifically, the term 'information' has specific, well-understood meaning that is different from what is taught in Wolff et al. With respect to the term 'information', it is respectfully believed that monitoring the value of a single signal line violates the commonly accepted meaning of the term information. For example, Merriam-Webster's online dictionary defines information as: '...the attribute inherent in and communicated by one of two or more alternative sequences or arrangements of something...' Wolff et al. merely compare two signal lines to see if they are the same, while being entirely unconcerned with the value of that signal line. So long as both signal lines are logic high or logic low, Wolff et al. will consider them a match. To consider the action of Wolff et al. to be acting upon information violates the meaning of the word information." The Examiner respectfully disagrees. The Examiner also consulted Merriam-Webster's dictionary and found that the missing part of the definition is as follows: "...the attribute inherent in and communicated by one of two or more alternative sequences or arrangements of something (as nucleotides in DNA or binary digits in a computer program)..." One of ordinary skill in the art knows that a binary digit in a computer program has one of two values, one or zero. Further, one of ordinary skill in the art knows that binary digits in a computer program are represented by either a logic high or logic low signal. The reference of Wolff et al. as stated by the Applicant compares signal lines and checks to see if they match—both logic high or both logic low. By the definition in Merriam-Webster's dictionary and Applicant's own admission, Wolff et al. does determine whether information in a packet satisfies one or more conditions.

14. On page 5, under the section A. Rejections under 35 U.S.C. 102, the Applicant argues, "Further, claims 1, 22, 33, and 34 call for a determination of whether the information in a packet satisfies one or more (emphasis added by Applicant) conditions. Because Wolff et al. compare a binary signal to another binary signal there is one and only one "condition" that can be satisfied. The Examiner respectfully disagrees. The claim, as written, is in the alternative; therefore only one condition has to be satisfied. Further, Wolff et al. satisfies more than one condition—both are logic high, both are logic low, or neither match.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Mon-Thu 7:30-5 and Fri. 7:30-4 (second Fri.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MM
April 1, 2003

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100